Differences to v7/AArch32 NEON

- **Syntax changes**
  - for example removing ‘V’ prefix (e.g. `VADD` => `ADD`), indicating data size and type with combined prefix and register type (e.g. `SMULL V0.2D, V1.2S, V2.2S`)
- **Existing instructions extended to support 64-bit integer values**
  - For example, comparison, addition, absolute value, negate
- **New instructions added**
  - For example, new lane insert and extract instructions, new data-processing instructions…
- **Registers**
  - 32 x 128-bit wide vectors instead of 16 x 128-bit vectors
  - 32 x 64-bit vectors held in the bottom 64 bits of each register
- **IEEE 754 floating-point standard support**
  - Support both **Single-precision (32-bit)** and **double-precision (64-bit)** floating-point vector data types operations
  - Increased support for IEEE 754, for example rounding modes and subnormals